REMARKS

Specification

The specification is objected to because the Abstract exceeds 150 words. The Abstract has been amended to overcome this objection. Applicant has also updated the status of the related applications.

Claim Objections

Claims 2-4, 7, 11-13, and 16 are objected to for minor informalities and have been amended in accordance with the Examiner's suggestions to correct the informalities.

Claims 5-9 and 14-18 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite. Claims 5, 7, 14, and 16 have been amended to overcome the rejection under 35 U.S.C. §112 and it is respectfully submitted, therefore, that the rejection of these claims, and the claims dependent therefrom, has been overcome. Dependent claims 9 and 18 have been canceled.

Claims 1-18 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,470,429 to Jones (hereinafter "Jones") in view of U.S. Patent No. 6,134,641 to Anand (hereinafter "Anand"). Applicant respectfully traverses the rejection of the pending claims. In the rejection of independent claims 1 and 10, Examiner correctly states that "Jones does not teach the bridge performing an uncacheable remote access to the cacheable coherent memory space of the first data processing system." Examiner then seeks to use Anand to supply a teaching of "using [an] uncacheable request to access a cache coherent memory space," citing column 5, lines 40-45 and column 9, lines 9-12.

Applicant respectfully submits that Examiner has engaged in an improper hindsight reconstruction of Applicant's invention. In this regard, Applicant notes that the actual feature recited in Anand is the "creation of a non-cacheable address block in normally cacheable system memory space" and this is accomplished by "setting up a virtual device." [Column 9, lines 3-5]. Anand teaches that this is accomplished as part of a four stage process:

> The first stage 210 comprises the step of setting up a virtual peripheral device in the computer system. The second stage 220 comprises the step of allocating a region in the computer system's

> non-cacheable address space to the virtual peripheral device. The third stage 230 comprises the step of allocating a region in the computer system's cacheable address space for the virtual peripheral device. Lastly, the fourth stage 240 comprises the step of mapping the range of non-cacheable address space to the range of cacheable address space such that accesses to the range of non-cacheable address space are automatically forwarded to corresponding addresses in the cacheable address space. [Column 5, lines 34-45 (emphasis added)]

Furthermore, the non-cacheable address block is implemented by "tricking" the operating system at boot-up.

> In step 320, upon reading the special configuration registers, configuration software will treat the special configuration registers as if they are identifying an actual peripheral device. Consequently, computer system 100 will be tricked to set aside system resources for virtual peripheral device 165 according to the contents of the special configuration registers. Significantly, the special configuration registers include a base address within a non-cacheable peripheral I/O address space such that the I/O addresses assigned to virtual peripheral device 165 will be non-cacheable. [Column 7, lines 21-29 (emphasis added)]

To establish obviousness based on a combination of elements disclosed in the prior art or a modification of the prior art, there must be some motivation, suggestion or teaching of the desirability of making the claimed invention. *See In re Dance*, 48 USPQ2d 1635, 1637 (Fed. Cir. 1998); *In re Gordon*, 221 USPQ 1125, 1127 (Fed. Cir. 1984). Whether the Office Action relies on an express or implicit showing of a motivation or suggestion to modify or combine references, it must provide particular findings related thereto. *In re Dembiczak*, 50 USPQ2d at 1617. Broad conclusory statements standing alone are not "evidence." *Id.* Thus, the Office Action must include particular *factual findings* that support an assertion that a skilled artisan would have modified the express disclosure of Jones using the Anand reference to develop the invention recited by Applicant's independent claims. *See In re Kotzab*, 55 USPQ2d 1313, 1317.

Applicant respectfully submits that a person of ordinary skill would not be motivated to modify Jones using the techniques taught by Anand. Examiner has made broad conclusory statements that one of ordinary skill in the art would "perform an uncacheable remote access to a cacheable coherent memory space, as is taught by Anand, in order for Jones' system to maintain coherency while avoiding bus snooping which results in improved performance." Applicant respectfully submits that Examiner has failed to meet the requirements of 35 U.S.C. §103(a) in

applying the combination of Jones and Anand as a basis for rejecting pending claims 1-8 and 10-16 and, therefore, the rejection of these claims should be removed.

In view of the remarks set forth herein, Applicants respectfully submit that all pending claims are in condition for allowance. Accordingly, Applicants request that the rejection of claims 1-8 and 10-16 be withdrawn and that a Notice of Allowance be issued. Nonetheless, should any issues remain that might be subject to resolution through a telephone interview, the Examiner is requested to telephone the undersigned at 512-338-9100.

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Respectfully submitted,

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